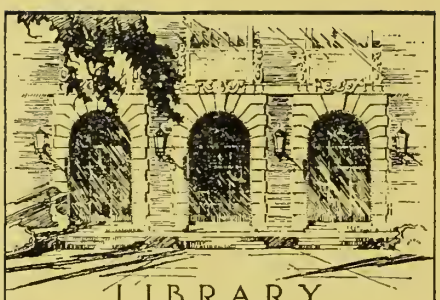

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URBANA, ILLINOIS

REPORT NO. 145

THE TRANSFER MEMORY

by

S. R. Ray

August 16, 1963

This work was supported in part by
Contract No. AT(11-1)-1018 of the Atomic Energy Commission

I. Introduction

The design of the ILLIAC III, a general-purpose information processing computer, calls for a specialized memory unit to mediate the flow of information from the primary processing logic (the "stalactite" array) to the control and bulk storage areas (the "control computer"). One operational function of this specialized memory unit, called the Transfer Memory (TM), is based on the disparity in word length between control computer words (32 bits) and stalactite words (1024 bits). The TM affords a high-speed means of word length conversion by allowing information to be read or written as either short words (32 bits) or long words (1024 bits). Bi-directional operation is the phrase used here to describe this property.[1]

It is also necessary that the TM be addressable on an information-content basis. This requirement, which is described in Section VI, arises from the need for rapid access to the typically few words in the TM proper which contain vital information. The addresses of such words can be determined only by information content, however.

The device which enables content addressibility, the Pyramidal Readout Encoder (PRE), is functionally distinct from the "Transfer Memory proper" and is, therefore, discussed separately. At the circuitry level, however, the PRE and TM partially merge.

II. General Design

A. Specifications

The general specifications of the Transfer Memory are as follows:

1. Size: 32,768 bits arranged in a 32 x 1024 matrix.
2. Operating Modes: Random Access, Parallel Read and Write Modes in either of two submodes:
   (a) Long Word Submode--the 32,768 bits arranged as 32 1024-bit words.
   (b) Short Word Submode--the 32,768 bits arranged as 1024 words of 32-bit length.

[1] The phrase "90° buffer" is also in occasional use with regard to row-column interchanges of information, especially with respect to punched cards.

It is necessary that the information in the Transfer Memory be readable in either submode independent of the submode in which the information was written. Briefly, the submodes must be compatible.

It is convenient to consider the TM "normal" configuration as 1024 32-bit words, in which case the short-word submode corresponds to a "parallel-by-word" operation while the long-word submode is a "parallel-by-bit" operation.

B. Basic Considerations

Magnetic cores were chosen as the basic storage elements of the TM. Their general availability, advantages for bi-directional operation, and ease of driving clearly overshadow the virtues of other components.

Operation in the long word submode for which 1024 bits must be handled is a particularly influential factor in establishing the design outlines. The 1024 sense amplifiers and digit drivers required by the long words constitute more electronics than a large, standard-variety computer memory. It is therefore proper to concentrate special effort on economy and reliability of these circuits.

For example, the number of turns of the sense windings is two rather than one in order to decrease the required sense amplifier gain and the digit current. The unusual shortness of the sense windings (32 bits) is also a substantial advantage in minimizing the recovery time of the lines, although it does not simplify the sense amplifier much. Destructive mode switching of the cores also provides relatively easily amplified signals at the cost of cycle time, of course.

It is possible to economize by using some drivers in two roles, either as "digit drivers" or as "write drivers" depending upon the submode.

C. Core Mode

The magnetic cores are operated in a nearly complete switching mode, that is 80 to 90 per cent of the flux is switched. This mode is attractive in a number of respects. An 80-90 per cent setting provides maximum signal amplitude per unit drive current (83 per cent

setting in some Mg-Mn cores).[2] The time for switching is substantially less than that required for complete switching (about 2/3) and the stability of the flux state approaches that of a completely switched core.

III. Organization

A. General

The general organization of the TM is recognizable as an elaboration of word-organized core memory techniques. Bi-directional operation complicates the terminology to the extent that a brief explanation is necessary.

Referring to Fig. III.1, during the READ portion of a memory cycle, the read drive is produced by the simultaneous operation of one of n read "source" drivers and one of m read "sink" drivers, where $n \cdot m \geq$ the number of words. The sense signals from the selected word are amplified and gated to the register or "buffer" flipflops. Rewriting of the buffer information occurs during the "WRITE" portion of the memory cycle. A "write driver" delivers current to the word which was previously read out. Simultaneously, the "digit drivers" (one driver per bit) are either turned on or remain off depending upon the state of their associated flipflop, i.e., upon the information just delivered from the cores in the case of a cycle for reading the stored information.

Note that the term "digit driver" is used in the sense of "the driver which is controlled by the buffer register during the writing portion of the cycle" and that the term "write driver" means "the driver which selects the word into which information is written." Specifically, these terms refer to the operational use of a driver during a given memory cycle, not to a particular physical circuit.

---

[2] Ray, S. R., "Engineering Model of a Partial Switching Effect in Ferrites," University of Illinois, Digital Computer Laboratory, Report No. 111, September 1961.

LRS - Long Word Read Source Driver
LRK - Long Word Read Sink Driver
SRS - Short Word Read Source Driver
SRK - Short Word Read Sink Driver
LWD - Long Word Write Driver
SWD - Short Word Write Driver
LS - Long Word Sense Amplifier
SS - Short Word Sense Amplifier
LB - Long Word Buffer Register
SB - Short Word Buffer Register
LA - Long Word Address Register
SA - Short Word Address Register

WL - Word Line Long
WS - Word Line Short
RL - Read Line Long
RS - Read Line Short

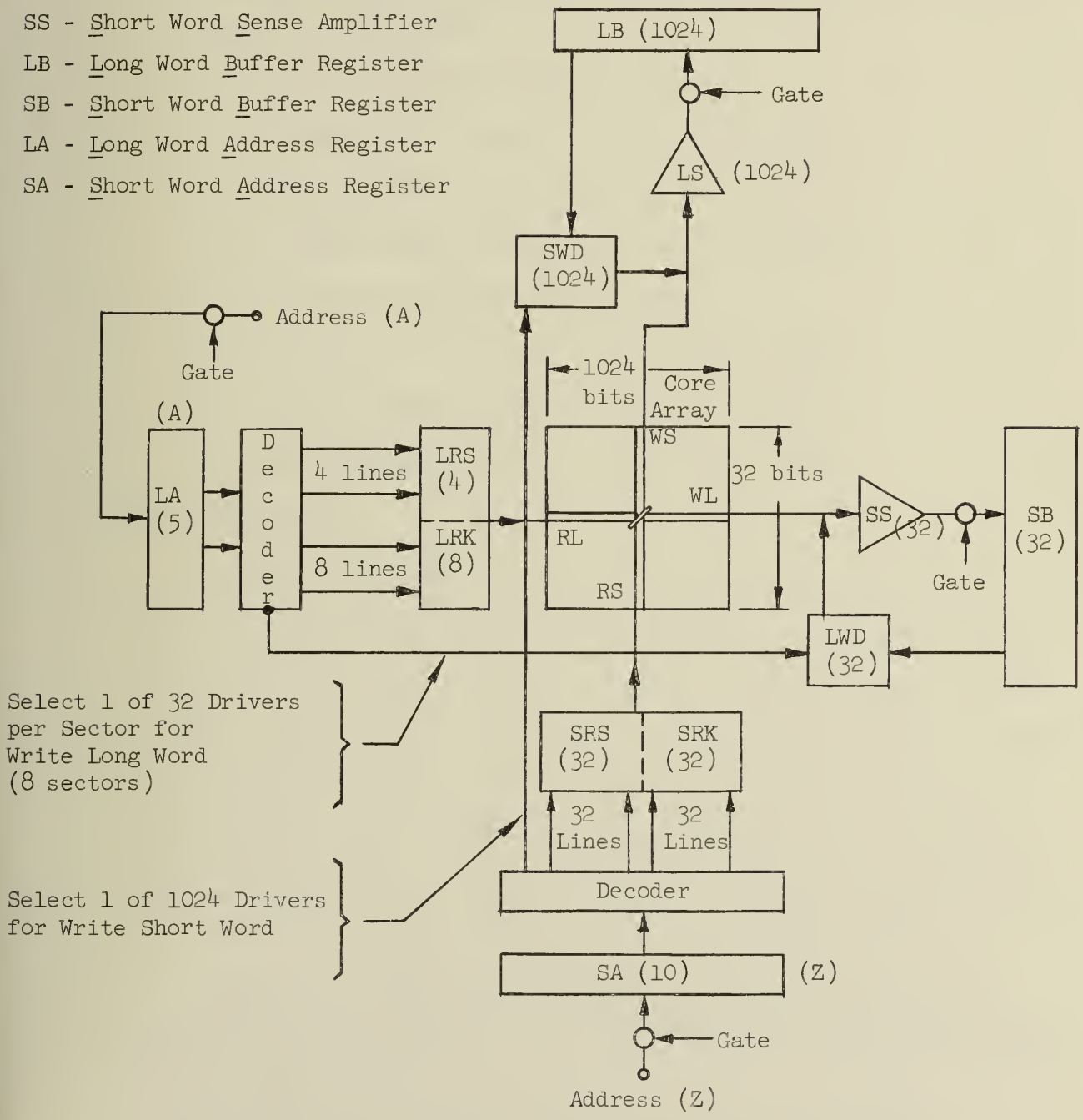


Figure III.1. Connection of Drivers and Amplifiers to Core Array

B. Core Matrix

The core matrix for the TM is arranged as eight planes of 32 x 128 cores per plane. Each core is linked by four windings as indicated in Fig. III.1 and named as follows:

1. Read Long Word Winding (RL)--1 turn--conducts the read current in long word submode.

2. Read Short Word Winding (RS)--1 turn--conducts the read current in short word submode.

3. Write Long Word Winding (WL)--1 turn

   (a) Conducts write current in long word submode.

   (b) Conducts sense signal in short word submode.

   (c) Conducts digit current in short word submode.

4. Write Short Word Winding (WS)--2 turns

   (a) Conducts write current in short word submode.

   (b) Conducts sense signal in long word submode.

   (c) Conducts digit current in long word submode.

C. Read Operations

The reading of long words is accomplished by selection of one of a set of four source drivers (an LRS-Long Word Read Source) and one of a set of eight sink drivers (an LRK-Long Word Read Sink) for each plane of the core matrix (see Fig. III.1). Each LRS driver delivers current through isolation diodes to the plus ends of eight RL windings. Each LRK driver absorbs current from the minus ends of one of four RL windings. This arrangement exists in parallel for each of the eight matrix planes, that is, eight separate but parallel-operated LRS and LRK driver sets exist, one set for each core plane, resulting in a total complement of 32 LRS drivers and 64 LRK drivers.

From this point of view, therefore, a 1024-bit-long word is operated as eight 128-bit words in parallel which appear concatenated at the system level.

The read mmf is 350-400 ma-t for some 300 nsec duration.

For short words, the read operation is performed by a source-sink arrangement as discussed above. Thirty-two SRS (Short Word Read Source) and 32 SRK (Short Word Read Sink) drivers are employed to select one of the 1024 short words.

The LRS and LRK drivers are identical in design to the SRS and SRK drivers, respectively.

Total requirements for read drivers are, therefore, 64 LRS-SRS circuits and 96 LRK-SRK.

D. Write Operations

The long word write windings (WL) are attached to the long word write drivers (LWD). Each sector of each long word is driven by a separate driver; therefore, there are 32 words x 8 sectors = 256 LWD's. The driver to be used in a write operation (actually eight drivers in parallel) are selected by a diode OR-AND circuit complex which is an extension of the long address decoder. The LWD delivers 120 ma into the one-turn WL winding. During short word operations, the LWD's operate as digit drivers under control of the short word buffer flipflops. Since the same amount of current is used for both write and digit drivers, no current selection network is required.

The short word write windings (WS) are similarly connected to the short word write drivers (SWD) which differ from LWD's only in the value of the output-current-determining resistor. The SWD current is 60 ma which produces an mmf of 120 ma-t, the same value delivered by LWD's, since the WS lines are two-turn windings.

One SWD is connected to each short word write winding for a total of 1024 SWD's. These also double as digit drivers in the long word submode.

E. Sensing

The sense signal peak amplitude has a nominal value of 30-35 mv per turn (for logical "1"), with a width of 160-180 nanoseconds. Hence, for long word operations where the two-turn WS winding delivers the sense signal, a 60-70 mv signal is expected as input to the Long Word Sense Amplifiers (LS).

The LS amplifiers have only one (two-wire) input each and deliver an amplified and strobed (gated) signal via 90-ohm coax to the M register.

The Short Word Sense Amplifiers (SS) are organized as eight preamplification sections followed by a common output circuit. For these amplifiers, the input signals which are delivered by the one-turn WL windings, are 30-35 mv peak amplitude.

The physical packaging of a large part of the sense amplifier circuitry is expected to be of the micropackaged "chip style" in which the elements lie on an insulating substrate.

IV. Some Circuit Matters

The logic circuitry for the TM is, in many respects, standard and therefore will not be discussed in detail.

The diagrams for the circuits discussed in the following sections are to be found in the appendix of this report.

A. Read Source Drivers (LRS-SRS)

The LRS and SRS drivers are required to pull up one end of a set of read windings. An NPN driver transistor is operated in the emitter-follower mode for this purpose. It is turned on by injecting base current from the secondary of the pulse transformer. Thus, the transformer secondary and the transistor base and emitter are all raised from -6 v to +30 v. Saturation is assured throughout most of the drive period in order to limit power dissipation in the transistor. Since only relatively few current sources are required, their power dissipation can be high without economic difficulty.

The read drivers are capable of delivering up to 400 ma for 400 nsec with a 1 μsec repetition time.

B. Read Sink Drivers (LRK-SRK)

The read sinks clamp down the negative ends of the read windings. When not selected, the 2N2219 collector is at +12 v. Upon turn-on of the 2N967, a current of about 400 ma is delivered by the 2N2219 which brings the collector to approximately +5 v. Since more current

is available from the sink than from the source, the collector will be solidly maintained at +5 v, and in a low-impedance condition.

Anti-saturation circuits are arranged for the 2N2219 so that cut-off will be relatively fast and yet the peak dissipation will not exceed one watt.

C. Write Drivers (SWD-LWD)

This is the driver circuit which appears in large quantity (1280) in the TM.

Basically, it can be seen that when the 2N967 turns on, the base current injected into the 2N2221 will cause the write winding (WS or WL) to be pulled down to about -30 v. The resistor marked R establishes the output current.

One compromise for economy is that no constant current source is provided. Therefore, the delivered current is a function of the non-linear reverse voltage of the write windings, that is, a function of the information being written. Tests indicate that this economy is feasible at the cost of extended write time. The substantial variations in writing current, it should be noted, make it imperative that the operating mode of the cores be stable in this respect.

A second compromise is also made in the cut-off of the 2N2221. It can be seen that statically, the $V_{be} = 0$ which is not as desirable, generally, as a small reversal of the base-emitter path. However, the backshoot of the transformer, during turn-off, assures fast action of 2N2221 while the steady-state external resistance in the V_{be} path, namely the transformer secondary, allows high V_{ce} voltages.

The input diode configuration is used to select the driver either as a digit driver (the a,b pair) or a write driver (the c,d,e triplet). The entire diode network is, therefore, an "AND-OR complex."

D. Sense Amplifiers

The final choice of the sense amplifier circuit configuration has not yet been made. The problems in this choice are decidedly severe due to:

1. the large number of components involved,

2. space limitation,

3. the problems of uniformity of the required number of circuits, and

4. all of the usual drift and gain control problems inherent in Class A amplification.

In order to reduce the volume of the circuitry as well as the labor in assembly, the possibility of micropackaging is currently being investigated. This style of packaging leads to further restrictions, especially of transistor polarity (NPN only) and number of pin connections. Also, there is a significant problem in establishing reliable information concerning the manufacturing limitations and controls. The costs involved are also more uncertain than for well-established construction techniques.

Nevertheless, the sense amplifier circuit specified as Mark II (see appendix) was evolved for micropackaging. Visibly, the circuit consists of two cascaded stages of direct-coupled differential amplification followed by an emitter-follower power amplification stage and strobing circuit. Signal polarity is such that "1" corresponds to a negative transition at the base of T_5. A special supply voltage is provided at point (b) in order to control the quiescent level of T_5's base. Point (b) is supplied by a special regulator whose output voltage tracks the +6 and -6 voltages, thus compensating for long term drift of the power supplies.

The high-frequency gain is controlled ($\pm$ 30 per cent) by the 20-ohm emitter resistors in the two initial stages, while the common mode gain is minimized by the relatively large emitter resistors (2 and 2.7 k).

The mid-range minimum differential voltage gain is approximately 100 which allows full output for a 25-mv signal. Upper frequency cut-off is in the vicinity of 3 mcps using 2N2222's.

A sense amplifier circuit which was used for test purposes is also given (Mark I). Other circuits suitable for micropackaging are being investigated.

V. Tests

A test model of the TM will be described in this section. The test model includes the following arrangements:

(1) 4 LRS, 8 LRK, and 32 LWD drivers to operate 32 long words of 128 bits length, effectively.

(2) 1 SRS, 32 SRK, and 32 SWD drivers to operate 32 short words.

(3) Associated counter, control logic and logic drivers.

Briefly, the model fully operates 32 bits of the 32 long words plus dummy operation of an additional 96 bits per word; also, 32 short words of 32 bits each are fully operated.

The core matrix which is used has 32 x 256 bits available. The cores are Electronic Memories Type 31-105, a 29-mil O.D., 20-mil I.D., 6.5-mil-high high-speed core.

The electronics described above occupies approximately 100 etched-wiring boards.

The described equipment provides adequate versatility to simulate worst conditions of the more troublesome sort. For example, variations in sense signal arrival time as a function of information pattern can be tested.

Some typical signals from the test model are illustrated in Fig. V.1. The sense amplifier in use was the Mark I version.

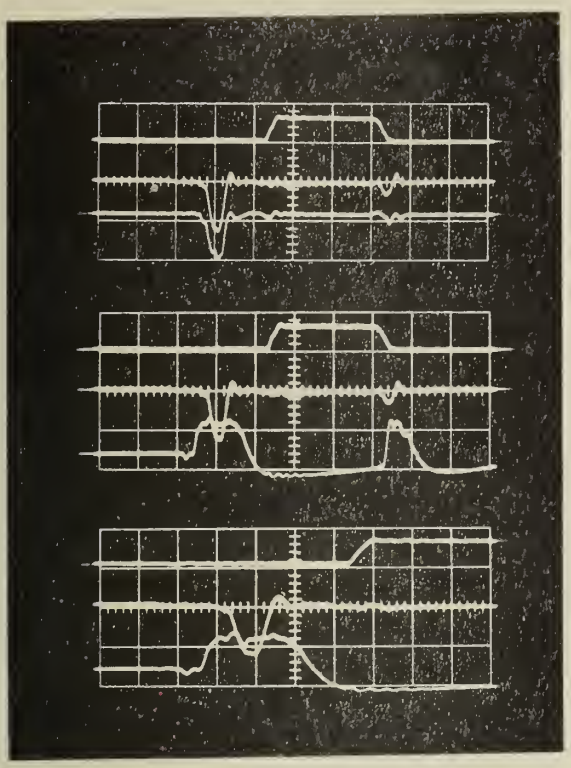
VI. The Pyramidal Readout Encoder

A. Functional Description

Consider the TM in the "normal" form of 1024 words of 32 bits each. A read operation in the long word submode then corresponds to a parallel-by-bit readout, after which one bit of all 1024 words exists in the M register of the PAU.

A bit containing "0" shall be said to be "marked" or that such a bit has a "jot" in it.[3] Given the M register as input, it is the

[3] A jot may represent a vertex point or road intersection point in pictorial information, for example.



Upper Photo

Horizontal:	200 nsec/cm
Upper Trace:	Digit Current in WS winding at 100 ma/cm
Center Trace:	Strobe
Lower Trace:	"1" output of sense amplifier

Center Photo

Horizontal:	200 msec/cm
Upper Trace:	Same as above
Center Trace:	Same as above
Lower Trace:	"1" single at base of penultimate sense amplifier transistor at 2 v/cm

Lower Photo

Same as center photo except horizontal scale is 100 nsec/cm

Figure V.1. Sample Signals from Test Version of TM Long Word Readout

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task of the PRE to deliver an output which uniquely describes the minimum bit number containing a jot, i.e., bit 2 in Fig. VI.1.

Bit Number:	1023	1022	...	5	4	3	2	1	0
M-Register Contents:	1	1	...	0	1	1	0	1	1

Figure VI.1

This PRE output must be in an encoded form suitable for communication to the TM address decoder, for example, a ten-bit address. The information thus encoded is the address (the "Z address") of the minimum word number in the TM which contains a jot in the particular bit under consideration. Upon signal from PAU control, it is then desired to read out the indicated word in TM for use by the control computer and to erase (i.e., set to "1") the jot in the M-register bit which was effective.

The foregoing description can be summarized as follows:

For the M-register flipflop outputs

$$M_i = 0 \text{ or } 1, \qquad i = 0, 1, 2, \ldots, 1023$$

Encode:

generate $\{Z_j\}$, $\quad j = 0, 1, \ldots, 9$

such that $\sum_{j=0}^{9} Z_j \cdot 2^j = k$ where

$k = \min(i)$ for which $M_i = 0$.

Read Marked Word:

Then, read word number k from the TM and

Erase Jot:

set $M_k = 1$.

In addition to these requirements, it also is desirable that the PRE operate with sufficient speed that the readout of successive short words, indicated by more than one jot in the M-register, proceed at the maximum cycle time of the TM. This requirement would be satisfied by a jot erasure and encode time no greater than 900 nanoseconds assuming a cycle time of 1.5 μsec.

B. Logical Design of the PRE Unit

The complete task of the PRE unit can be considered as the three independent operations, encoding, reading the marked word, and jot erasure as indicated in the preceding section. Since the "read marked (short) word" is a normal operation of the TM, however, only the encoding and jot erasure need special attention.

1. The Encoder

The most economical design of the encoder which has been found so far will be described.

We consider the problem of generating a set of signals,

$$\{x_i, y_j\} \qquad i,j = 0,1,\ldots,31$$

such that a unique x, x_p and a unique y, y_q are true, and represent the minimum jot location in the familiar form $k = 32q + p$ where M_k is the minimum marked flipflop. It is then a straightforward matter to produce a ten-bit address.

Consider the simpler case of 16 M-register flipflops and arrange these in a 4 x 4 array as in Fig. VI.1.

y	M_{12}	M_{13}	M_{14}	M_{15}
	M_8	M_9	M_{10}	M_{11}
	M_4	M_5	M_6	M_7
	M_0	M_1	M_2	M_3
		x		

Figure VI.1

An example case is shown in Fig. VI.2 with M_6, M_9, and M_{15} having jots.

	x_0	x_1	x_2	x_3
y_3	1	1	1	0
y_2	1	0	1	1
y_1	1	1	0	1
y_0	1	1	1	1

Figure VI.2

In this case we should arrive at true signals for y_1 and x_2 since k = 6. Some examination will show that the solution (in general) may be described diagramatically as follows: find the row nearest the bottom which contains at least one zero; then for the elements of that row, find the left-most column which contains zero.

Drawing C-3095[4] is the diagram of the logic which would accomplish the task described, the z signals being the encoded address. When extrapolated to the case of 1024 inputs, the only difficulty which arises is the time required to propagate a "carry" in the priority circuits. The standard technique of breaking the carry chain into shorter segments can be applied, resulting in an encoding time of 20 circuit transitions or less, that is 800 nsec at 40 nsec per circuit. This time can be reduced by 25 per cent or more with negligible increase in cost, by specializing the circuit design and using the ultimate minimum carry chain.

The existence or nonexistence of a jot in the M-register is indicated by the "some mark" signal.

[4] See Appendix.

The diode-transistor cost of the encoder is roughly 4,500 diodes and 600 transistors. The relatively low transistor count is accomplished by maximum use of diode logic which, however, corresponds to a load of perhaps 12 ma on the $\overline{M}_i$ signals.

2. Erasure Circuits

The erasure circuits generate a full decoding of a 10-bit address, that is, one of the 1024 outputs is "1." The address will always be the contents of the short word address register (SA) of the TM, which must be decoded in any case. Thus, the erase circuits coexist, in part, with the short address decoder of the TM, delivering their output to the M register. The arrangement described, diagrammed in Fig. VI.3, allows the following basic variants of addressing, reading, and erasing:

1. a. Gate Address (Z) from PRE to Short Address Register, or

   b. Gate Address (Z) from Control to Short Address Register

2. For either address of part 1:

   a. Read the indicated short word only, or

   b. Read the indicated short word and erase the corresponding M-register bit, or

   c. Erase the M-register bit only.

Successive 1a, 2b micro-operations, for example, would correspond to reading sequentially all short words corresponding to jots in the M register. The 1b, 2c micro-operations, followed by complementing the M register, could establish a jot at the address specified by an instruction address.[5]

The diode-transistor count chargeable to erasure circuits is 1,300 transistors and 3,100 diodes. It is conceivable that these figures can be improved. The total time required for operations 1a or 1b and 2c is estimated at 200 nsec.

[5] This operation would be used, typically, to set up the starting point of a path readout in pictorial information.

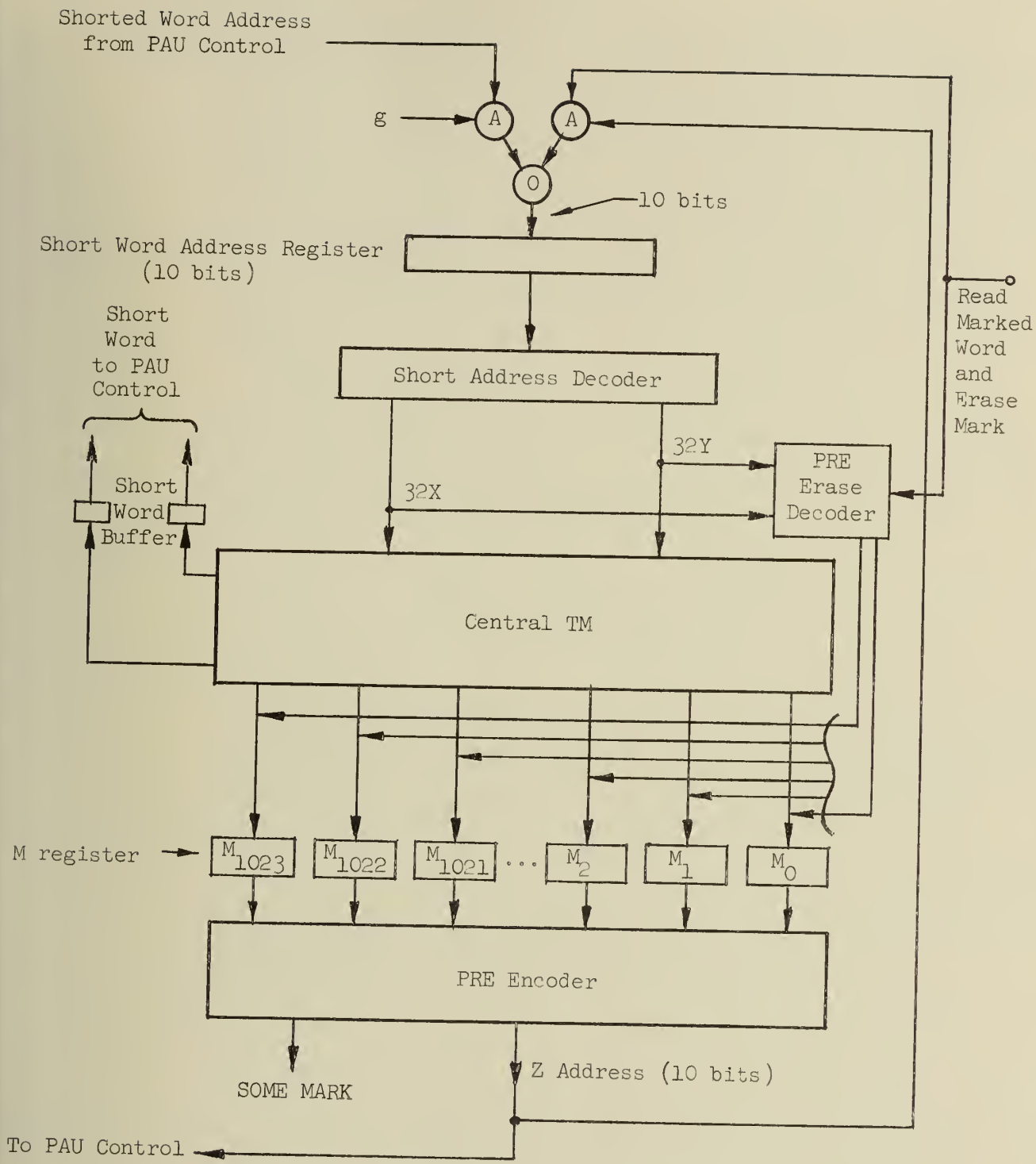


Figure VI.3. PRE Encoder and Erase

3. Content-Addressable Operations

Assume a specified set of bits of all 32-bit words is considered to constitute a tag. These bits may be read from the TM into the PAU in the parallel-by-bit (or long word) submode. In the PAU, any desired logical operations may be performed, with programmed control, on the tag bits. The set of words whose tags meet the programmed criterion could then be read from the TM or, alternatively, only the addresses of such words. The case of a vacuous set would be indicated by falsity of the "some mark" signal.

The mechanism described, therefore, allows tags of 1 to 32 bits to be employed. It is also interesting to note that since any singlet, pair, triplet, etc., of bits may be used as tag, the number of possible tag arrangements is:

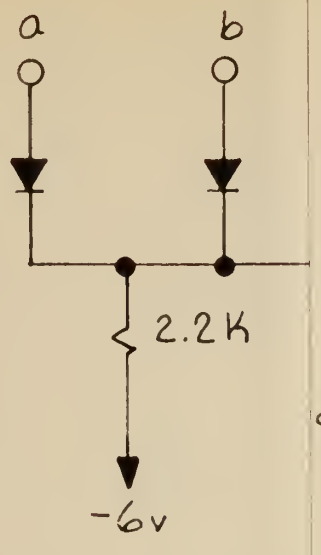
$$\sum_{k=1}^{32} 2^k \cdot \frac{32!}{k!(32 - k)!}$$

If this statement appears to defy information theoretic laws, it is because part of the information, namely, the knowledge of which bits are to be taken as the tag, does not exist in the transfer memory but in the programmer's memory.

The combination of transfer memory, pyramidal readout encoder, PAU and associated control may be considered as a versatile, if somewhat bulky, associative memory of 1024 words.

APPENDIX

1. Drawing: SRS-LRS
2. Drawing: SRK-LRK
3. Drawing: SWD-LWD
4. Drawing: Sense Amplifier--Mark 1
5. Drawing: Sense Amplifier--Mark 2
6. Drawing C-3095 (PRE: Pyramidal Readout Encoder)



WHEN NOT SPEC

RESISTORS 1/4
RESISTORS ±5%
DIODES TI-252
T = STANDARD

NOTES:

INPUT SIGNALS:
1. GUARANTEED CUT "OR RS"
2. " CONC

FOR "LRS":

$a = \overline{lami}$

$b = \overline{sami}$

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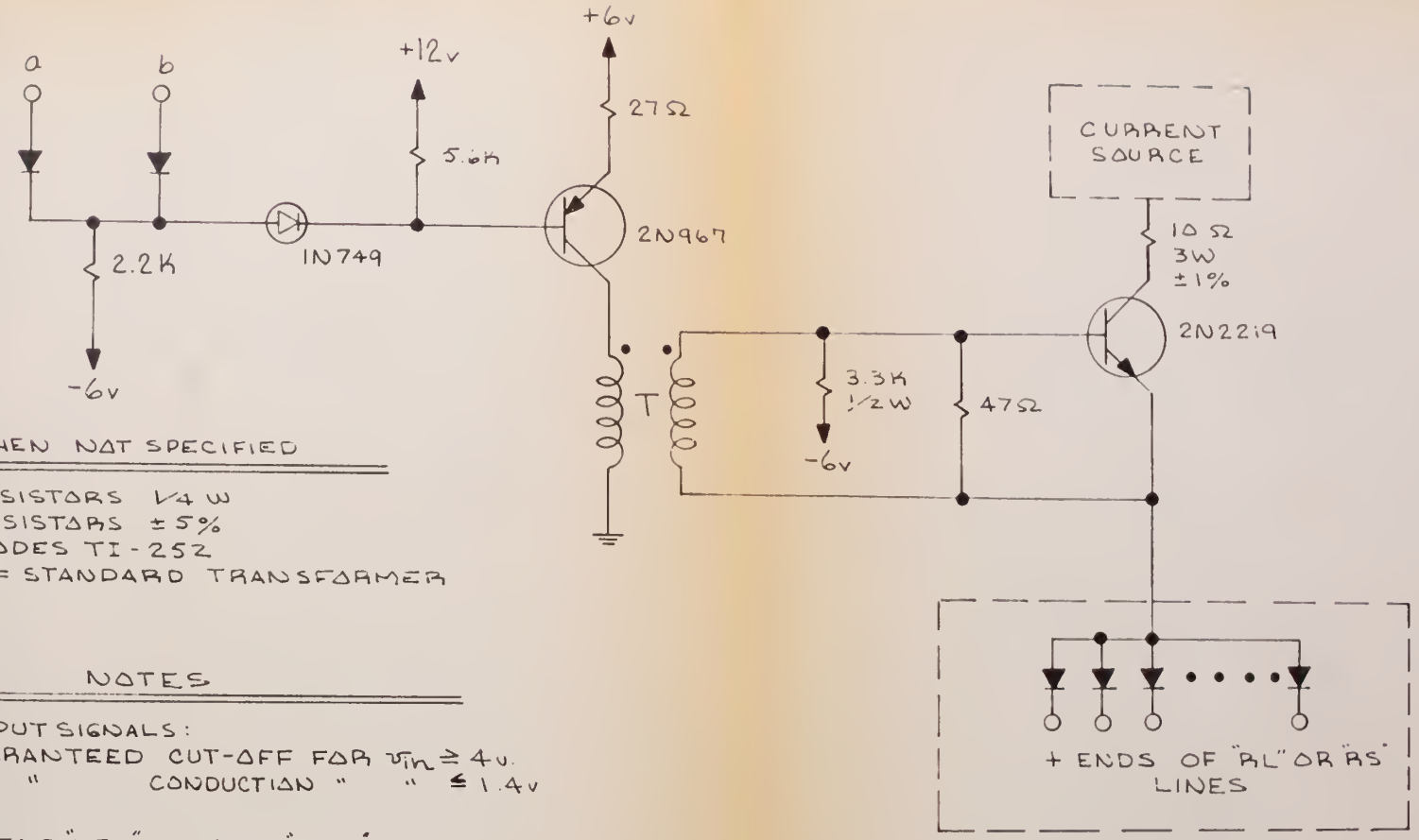
FOR S.R. BY K.C.L. CH

APP. _____ & _____



WHEN NOT SPECIFIED

RESISTORS 1/4 W
RESISTORS ±5%
DIODES TI-252
T = STANDARD TRANSFORMER

NOTES

INPUT SIGNALS:
1. GUARANTEED CUT-OFF FOR $v_{in} \geq 4v$.
2. " CONDUCTION " " $\leq 1.4v$

FOR "LRS":	FOR "SRS":
$a = \overline{lami}$	$a = \overline{SWO \cdot ROT}$
$b = \overline{sami}$	$b = \overline{LWO \cdot ROT}$

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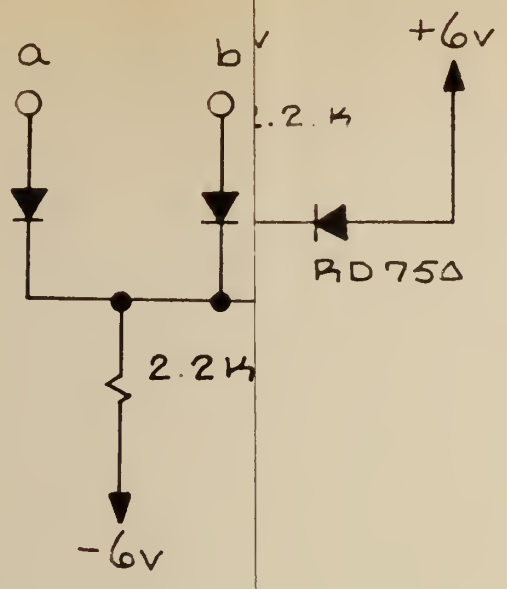
FOR S.R. BY K.C.L. CHK'D S. Ray APP _____ & _____ 1-26-63	TRANSFER MEMORY LRS - SRS DRIVERS

S" OR "RL" LINES



FOR "LRK WHEN NOT SPECIFIED

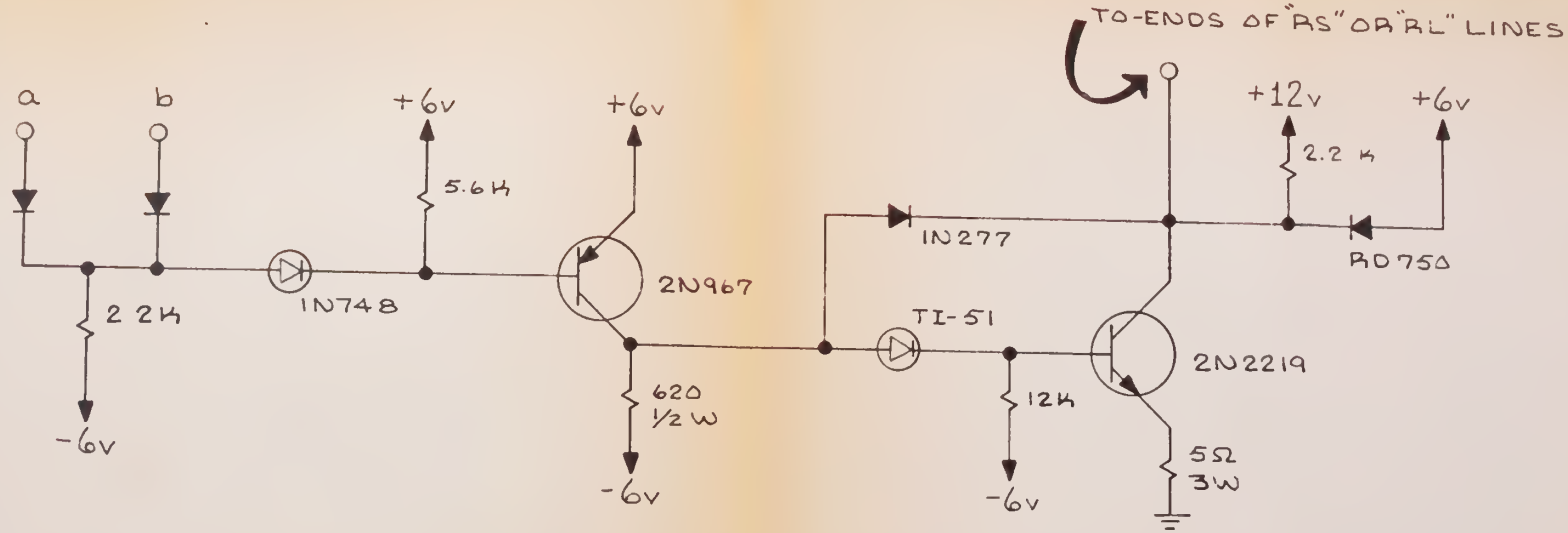
$a = \overline{la}\,\overline{lj}$

$b = \overline{LWO \cdot R}$

ESISTORS 1/4 W
ESISTORS ±1%
IODES TI-252

1. GUARANTE
2. "

UNIVERSITY o RATORY	
FOR S.R. BY K.C.L (	
APP. &	



FOR "LRK":

$a = \overline{lalj}$

$b = \overline{LWO \cdot ROT}$

FOR "SRK":

$a = \overline{salj}$

$b = \overline{SWO \cdot ROT}$

WHEN NOT SPECIFIED

RESISTORS ¼ W
RESISTORS ±1%
DIODES TI-252

NOTES

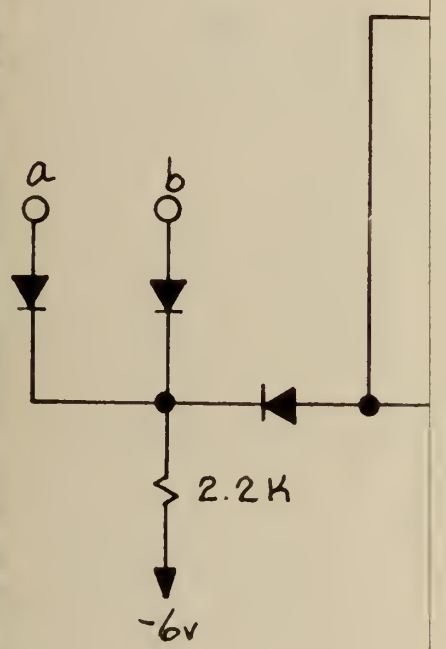
1. GUARANTEED CUT-OFF FOR INPUT VOLTAGE ≥ 4.1v
2. " CONDUCTION " " " ≤ 1.7v

UNIVERSITY of ILLINOIS - GRADUATE COLLEGE - DIGITAL COMPUTER LABORATORY		
FOR S.R. BY K.C.L CHK'D S. Barry APP. _____ & _____ 1-25-63	TRANSFER MEMORY SRK - LRK DRIVERS.	

WHEN NOT SPECIFIED

ESISTORS 1/4 W
ESISTORS ± 5%
T = STANDARD TRANSFORMER
DIODES TI-252

	FOR "LWD"	FOR "SWD"
R =	260Ω, 3W, ± 1%	520 Ω, 3W ± 1%



	FOR "LWD"	FOR "SWD"
a =	$\overline{SWO \cdot WOT}$	$\overline{LWO \cdot WOT}$
b =	$\overline{swb_i}$	$\overline{lwb_i}$
c =	$\overline{LWO \cdot WOT}$	$\overline{SWO \cdot WOT}$
d =	$\overline{lam_i}$	$\overline{sam_i}$
e =	$\overline{lal_i}$	$\overline{sal_i}$

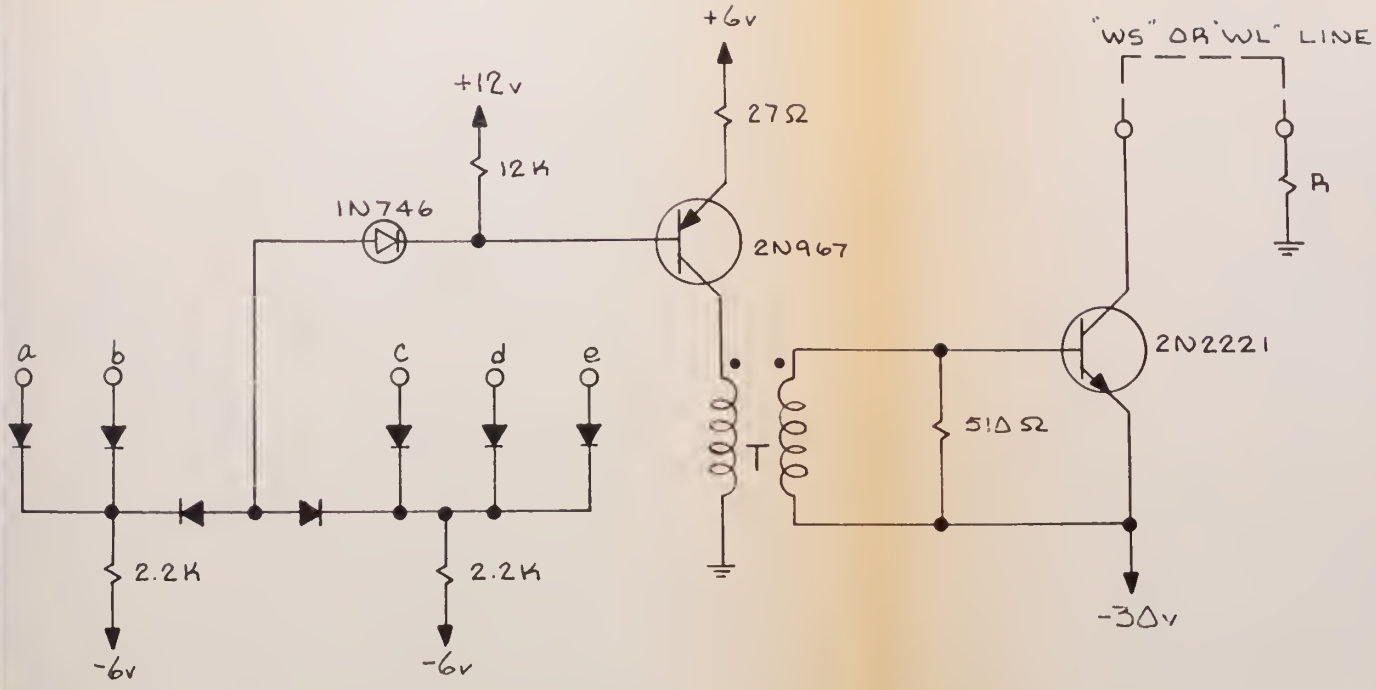
1. MAX. INPUT G
2. MIN. "
3. MAX. REQUIRE

UNIVERSITY of ATORY

FOR S.R. BY KCL. C
APP. _____ & _____

WHEN NOT SPECIFIED

RESISTORS 1/4 W
RESISTORS ± 5%
T = STANDARD TRANSFORMER
DIODES TI-252



	FOR "LWD"	FOR "SWD"
R =	260Ω, 3W, ± 1%	520Ω, 3W ± 1%

	FOR "LWD"	FOR "SWD"
a =	$\overline{SWO \cdot WOT}$	$\overline{LWO \cdot WOT}$
b =	$\overline{swbi}$	$\overline{lwbi}$
c =	$\overline{LWO \cdot WOT}$	$\overline{SWO \cdot WOT}$
d =	$\overline{lami}$	$\overline{sami}$
e =	$\overline{lali}$	$\overline{sali}$

NOTES

1. MAX. INPUT GUARANTEED TO CAUSE TURN-ON = 1.5v
2. MIN. " " " " CUT-OFF = 4.5v
3. MAX. REQUIRED INPUT CURRENT = 5.74 ma.

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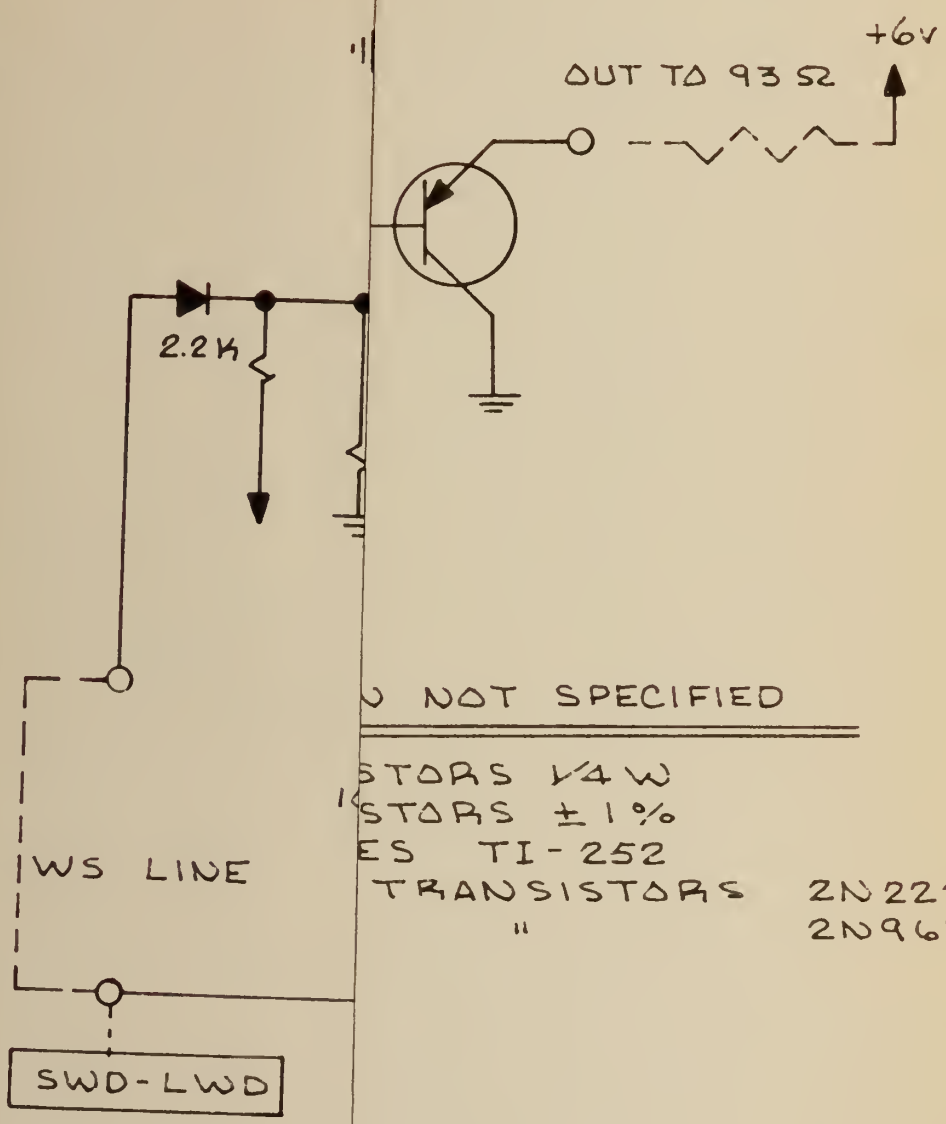
FOR S.R. BY KGL. CHK'D S. Ray
APP. _____ & _____ 1-25-63

TRANSFER MEMORY
LWD - SWD DRIVERS



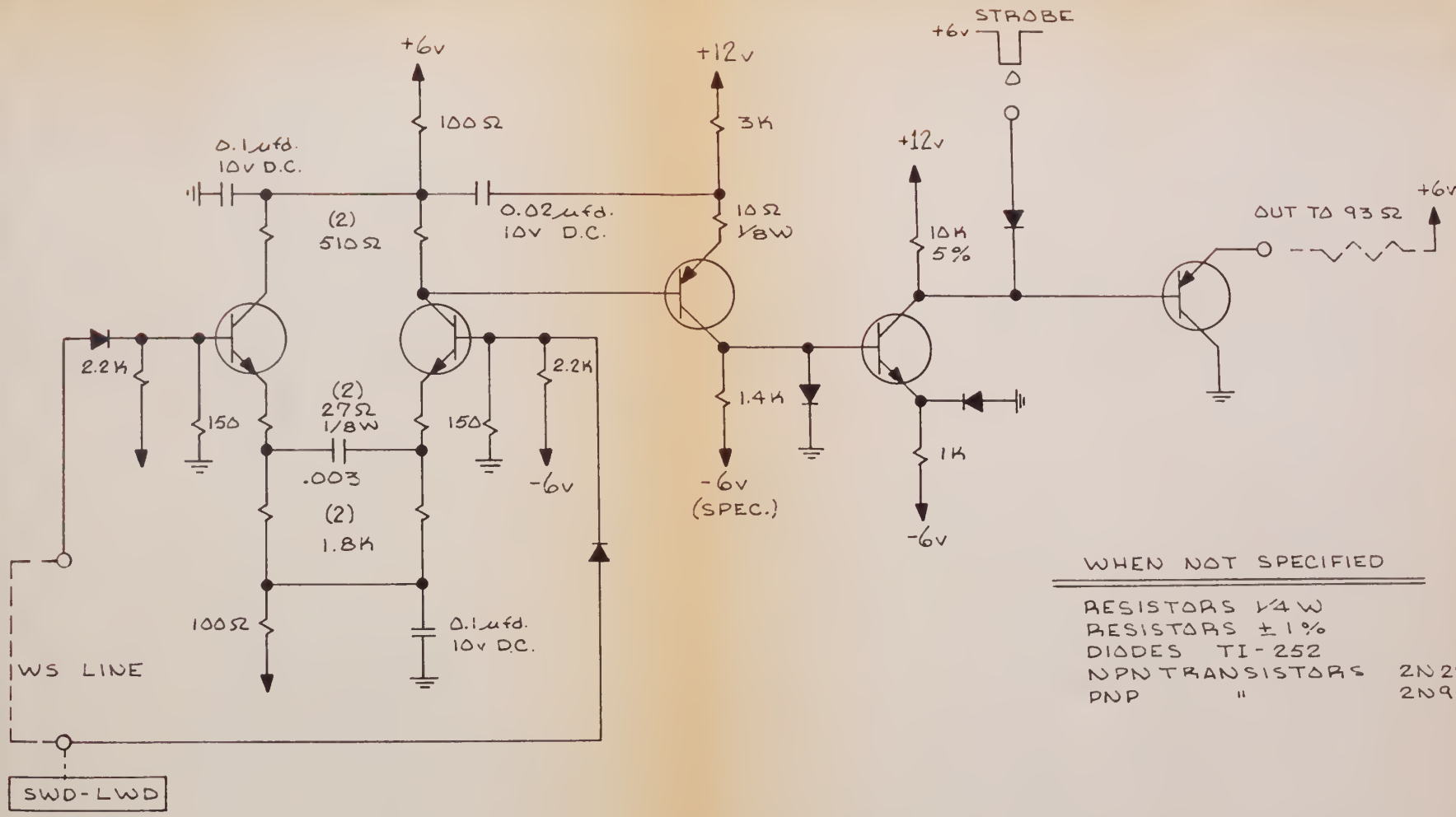
NOT SPECIFIED

STORS 1/4 W
STORS ± 1%
ES TI-252
TRANSISTORS 2N2222
" 2N967

UNIVERSITY oRATORY

FOR S. R. BY K.C.L.

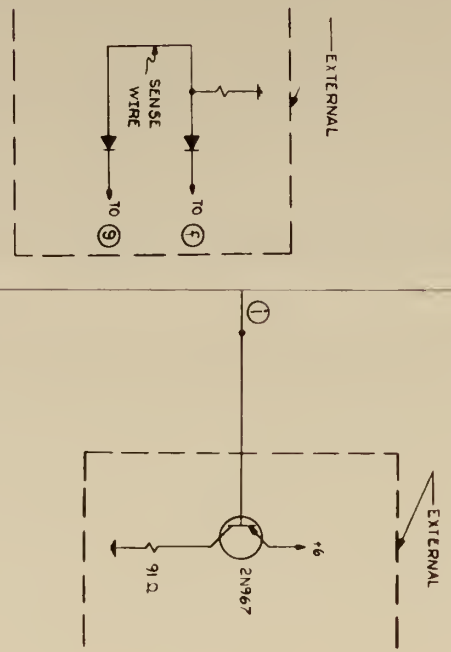
APP. _____ & _____



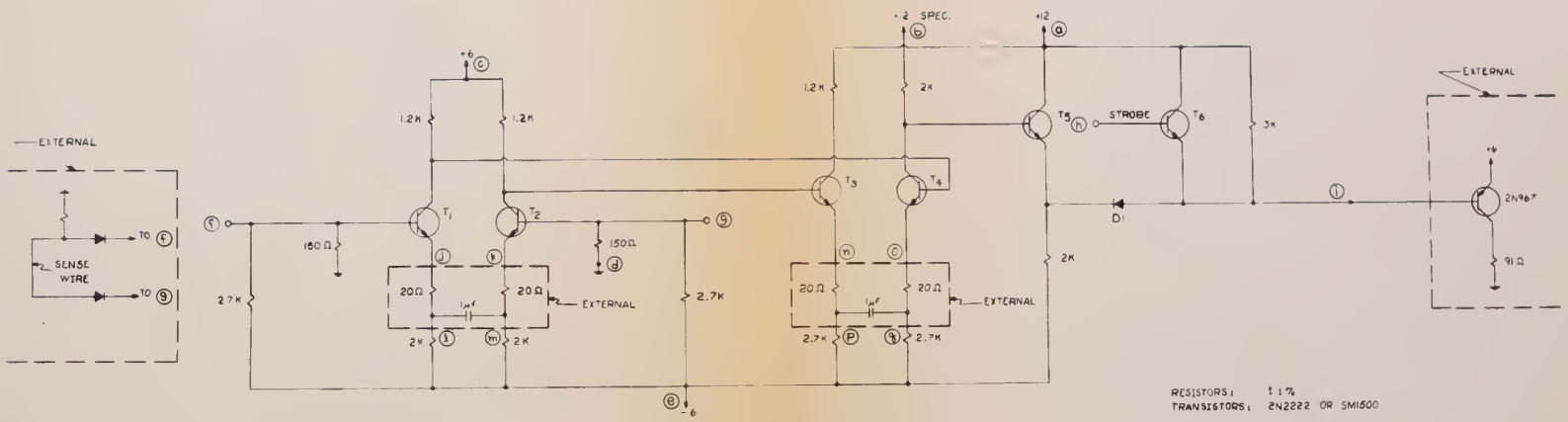
WHEN NOT SPECIFIED

RESISTORS 1/4 W
RESISTORS ± 1%
DIODES TI-252
NPN TRANSISTORS 2N2222
PNP " 2N967

UNIVERSITY of ILLINOIS - GRADUATE COLLEGE - DIGITAL COMPUTER LABORATORY		
FOR S. R. BY K.C.L. CHK'D S. Ray APP. _____ & _____ 1-4-63	TRANSFER MEMORY SENSE AMPLIFIER (MARK I)	



UNIVERSITY of ILLINOIS - GRADUATE COLLEGE - DIGITAL COMPUTER LABORATORY		
FOR SR BY EDC CHK D APP _____ & _____ 3-13-63	SENSE AMPLIFIER (MARK II)	C-3305



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SENSE AMPLIFIER (MARK II)

C-3305

FOR SR BY EDC CHK D 3-13-63
APP &

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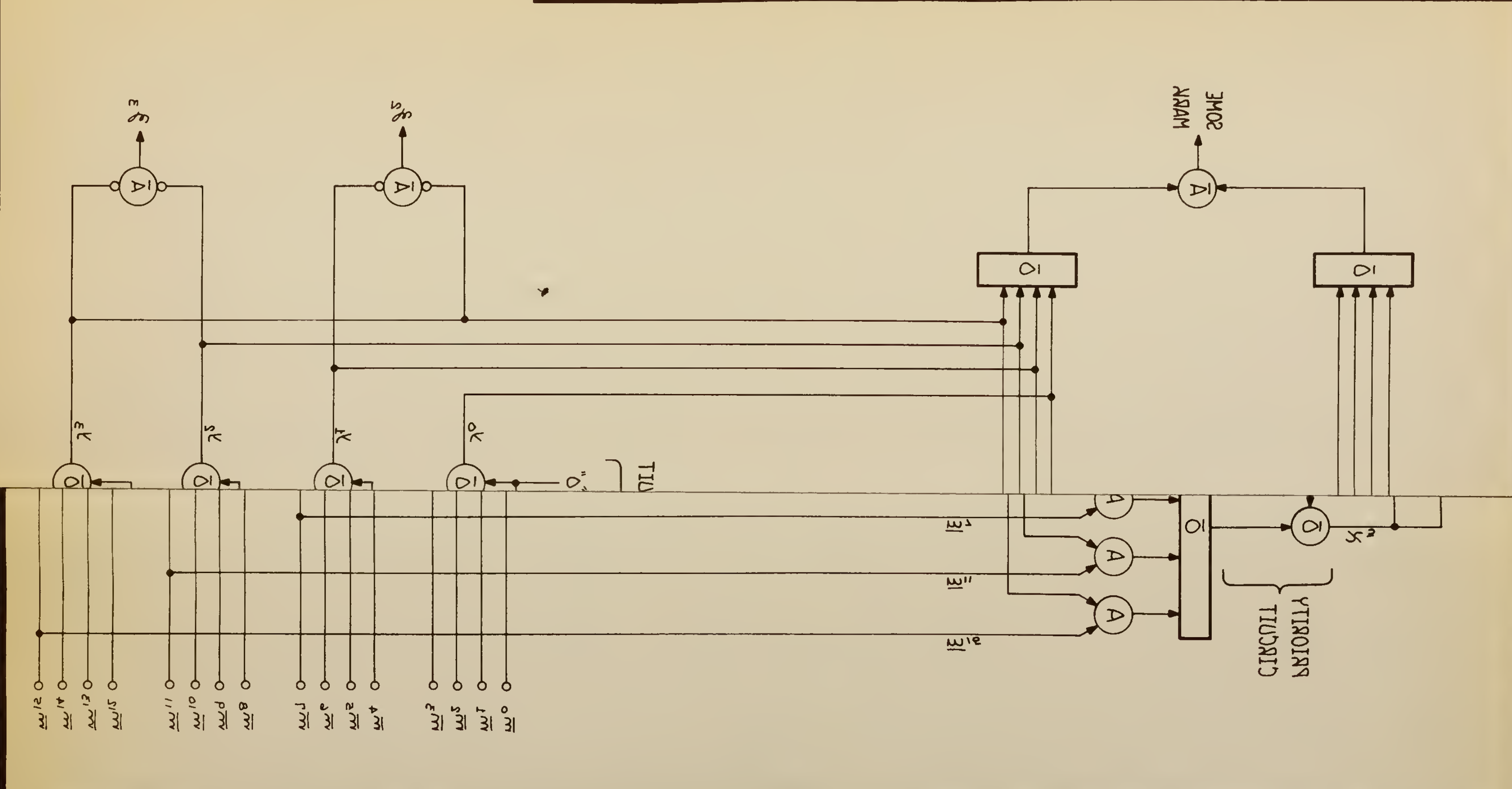
FOR S.RAY BY KCL CHK D.S.R. 7-24-63

APP 8

PRE UNIT ENCODER (SUBUNIT)

C-3095



UNIVERSITY OF ILLINOIS - GRADUATE COLLEGE - DIGITAL COMPUTER LABORATORY
SHIFT UNIT ENCODER (12BUS)
C-3082
CHK
DWN
CIRCUIT
VARIATION
SMOS
ARAM

JUN 20 1989

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